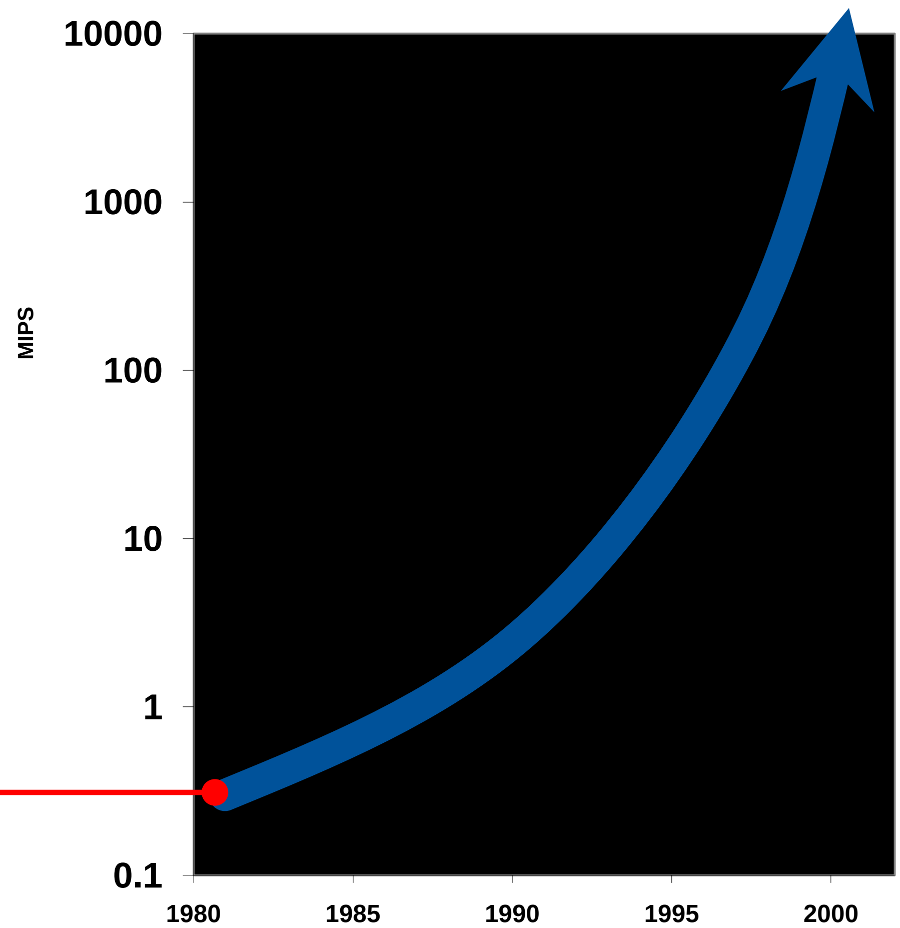
NATIONAL INSTRUMENTS™

Real-time Noise Source Identification System Using Reconfigurable Field Programmable Gate Array Technology

Chris Fronda, Product Manager

Leveraging Advances in Technology

- 1981
- 4.77 MHz
- 64 kB RAM
- 5.25" FD, 160 kB
- Monochrome
- $3,000



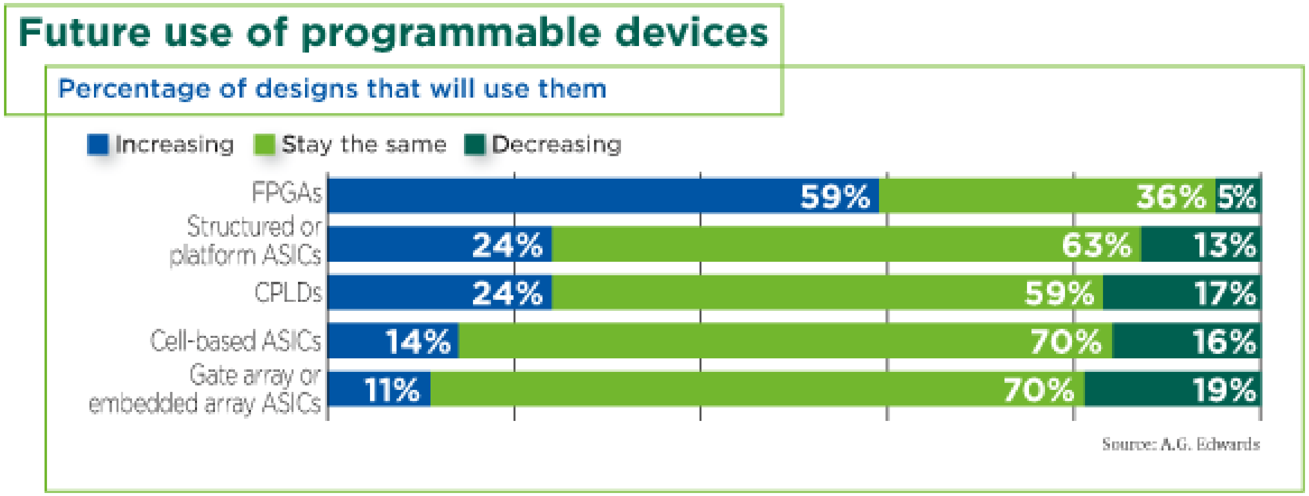
- 2007
- 2.0 GhZ Dual
- 2GB RAM
- 120 GB HD
- 48X CDRW
- 1 GB Ethernet
- XGA, 64 MB
- $1,400

Industrial Embedded Processors

- High Performance 16/32-bit Processor enables next generation embedded applications
- Easy to use Tools Increases developer productivity

Analog Devices
Texas Instruments
Freescale

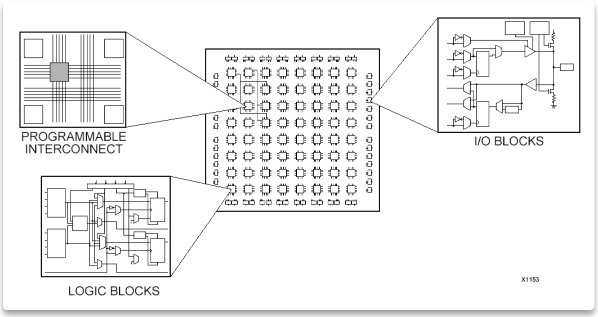
FPGAs: Another Embedded Processor



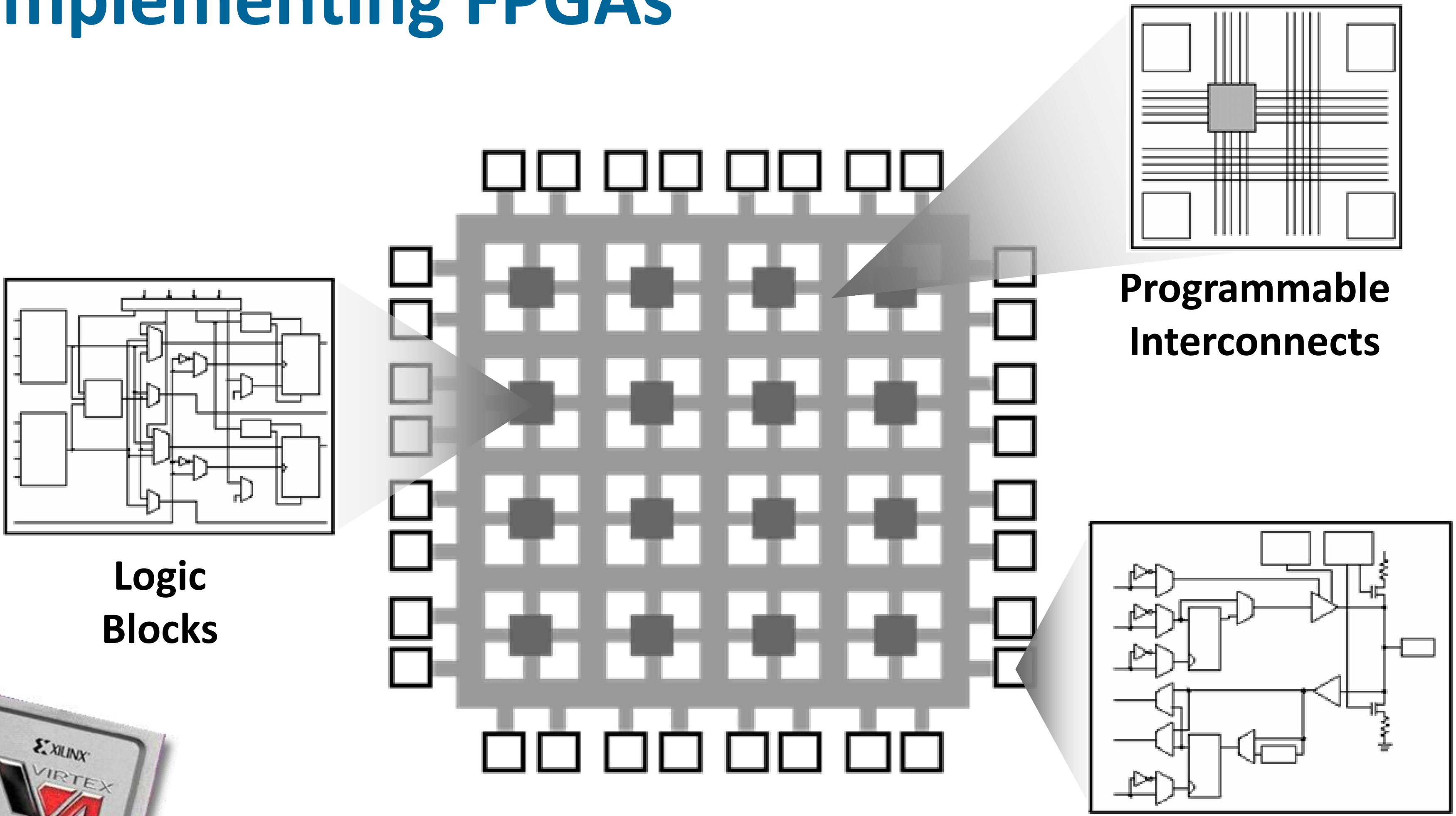
- Reconfigurable
- True parallelism
- High Determinism
- Independent operation
- Unique functional cores or IP cores

What is an FPGA?

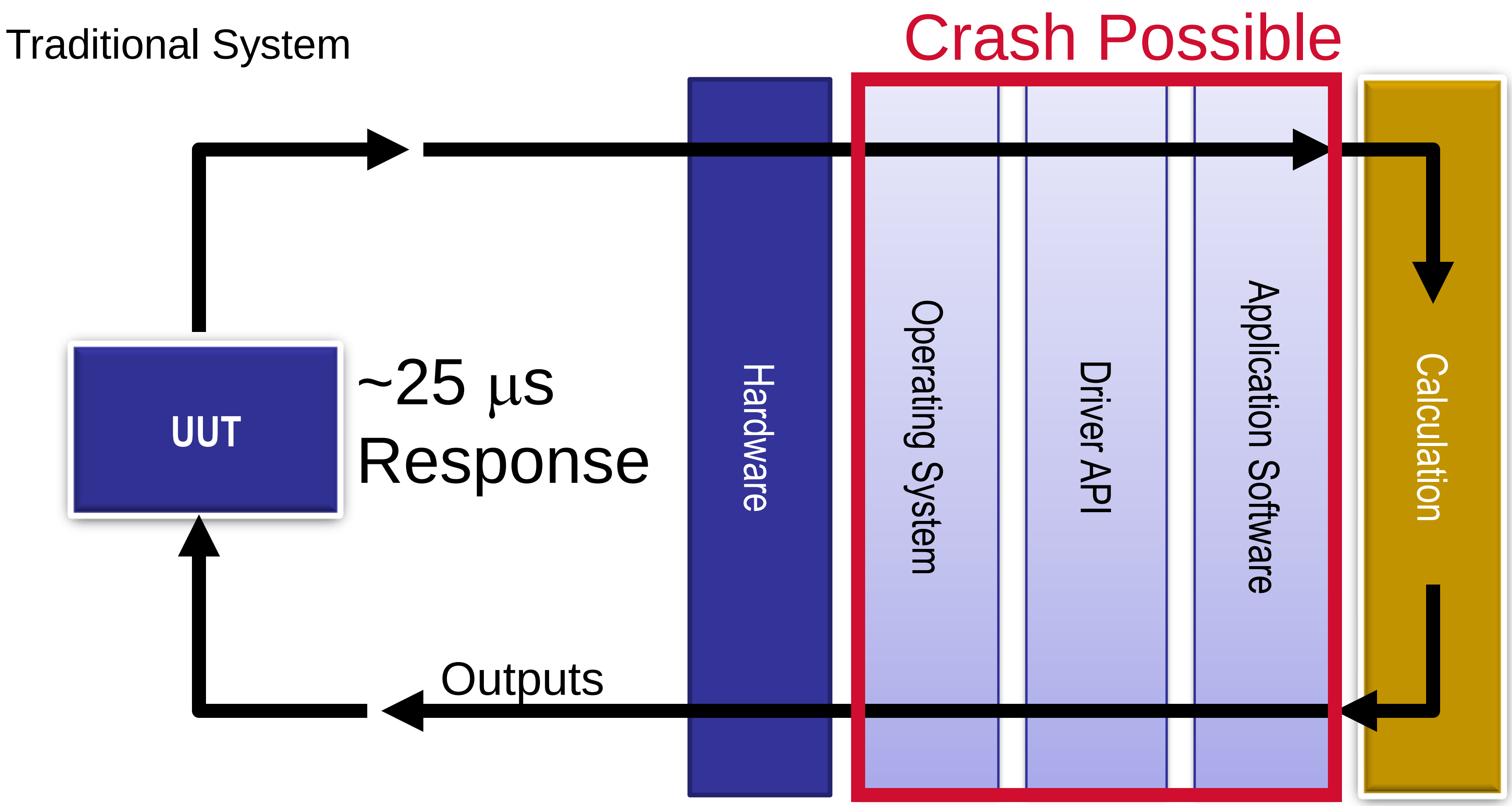
- **What it is**
  - Field-programmable gate array
  - A silicon chip with unconnected gates
  - User can define and re-define functionality
- **How it works**
  - Define behavior in software
  - Compile and download to the hardware
  - Hardware implementation of code



Implementing FPGAs

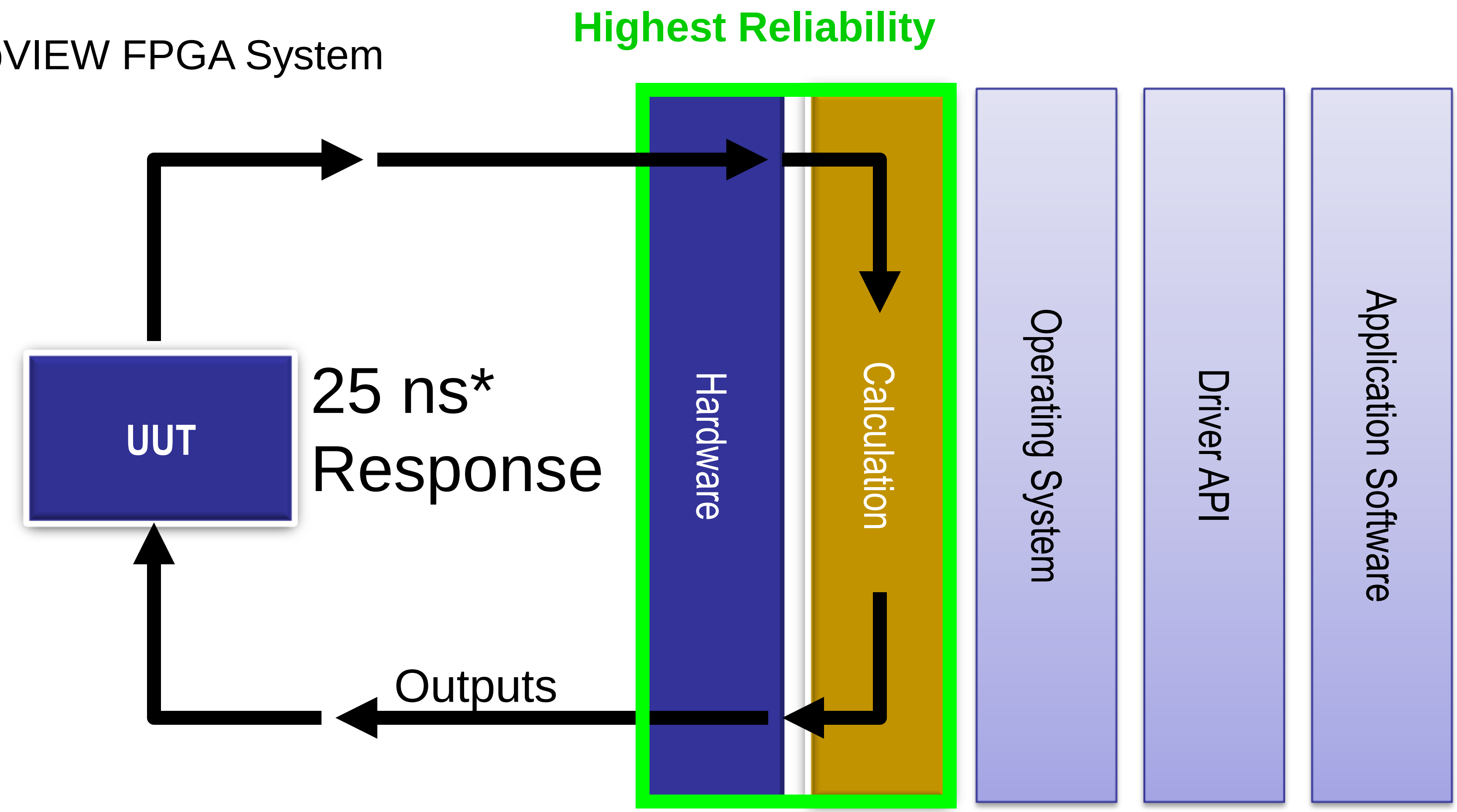


Decision Making in Software



Decision Making in Hardware

LabVIEW FPGA System



* Faster response for 80 and 120 MHz clocks

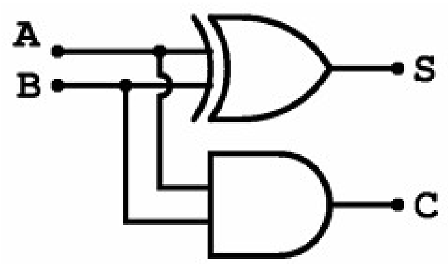
VHDL Framework & Syntax

- VHDL Description of Logic Blocks is split into
  - **Entities**
    - Defines the **Inputs** & **Outputs** of a design
    - Similar to a **declaration** of a function in C, C++
  - **Architecture**
    - **Describes** the **logic** behind the entity
    - Similar to a **description** of a function in C, C++

VHDL Example: 1-Bit Adder

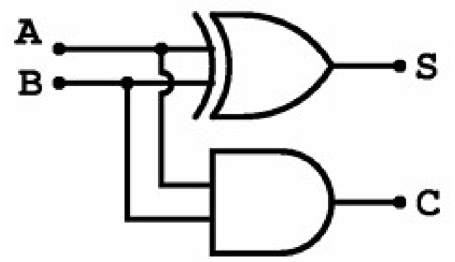
library ieee;
use ieee.std_logic_1164.all;

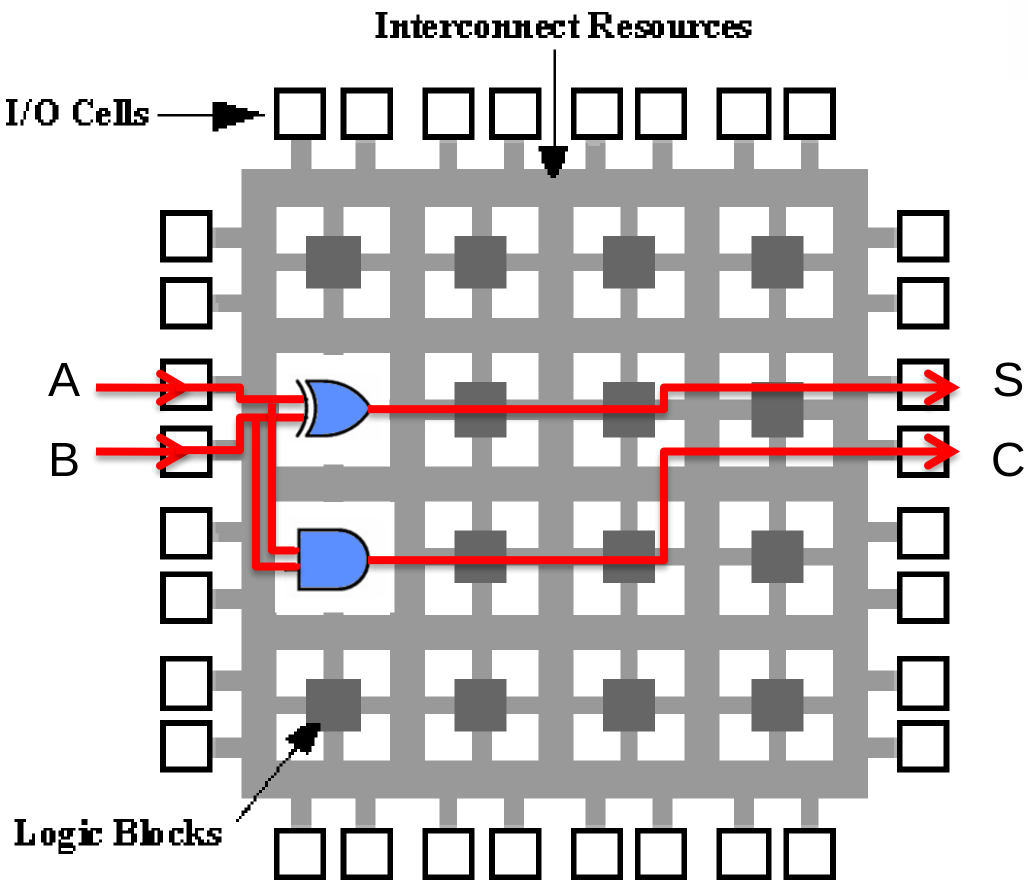
ENTITY **Single_Adder** IS PORT
(
    A, B: IN std_logic ;
    S, C: OUT std_logic
);
END Single_Adder;



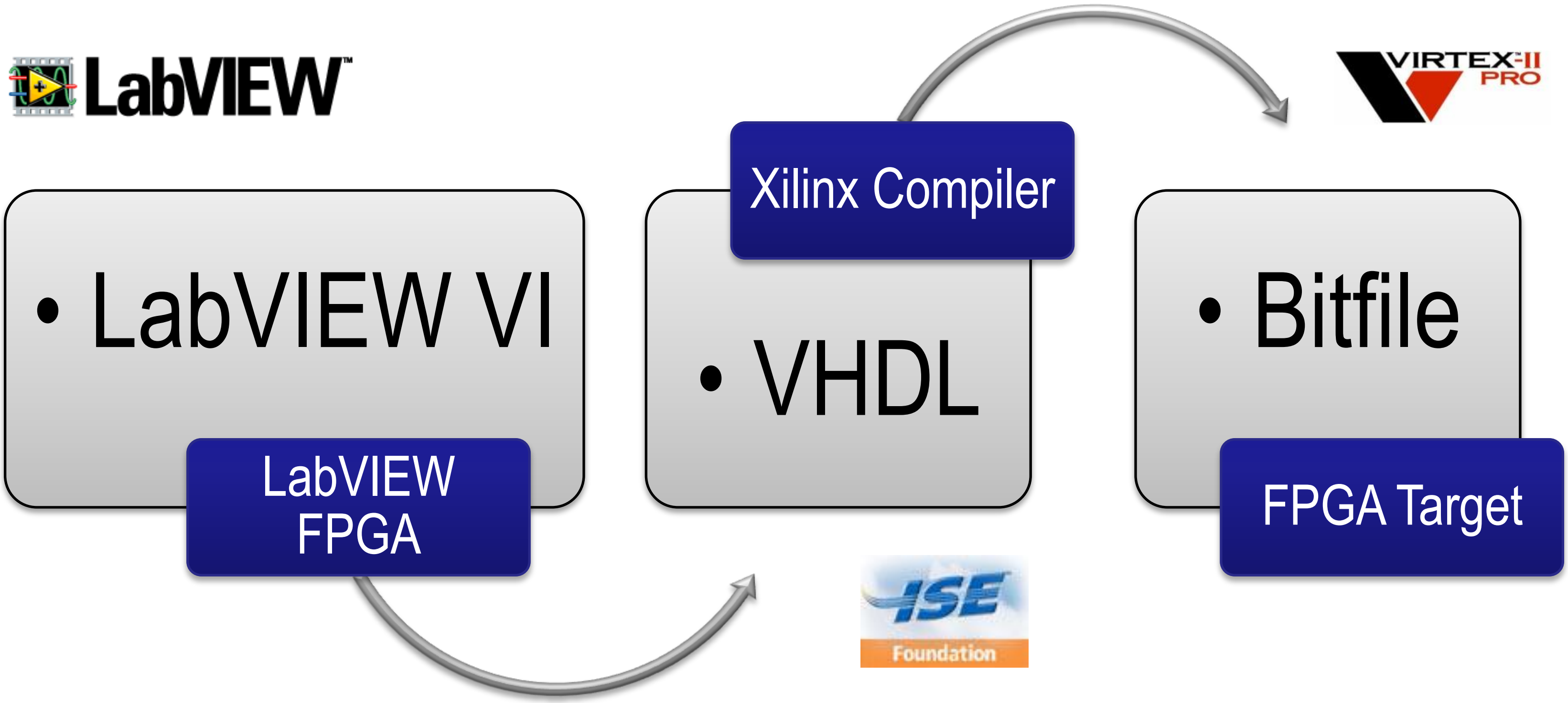
ARCHITECTURE Architecture_Single OF **Single_Adder** IS
BEGIN
    S < = A xor B;
    C < = A and B;
END Architecture_Single;

FPGA Implementation



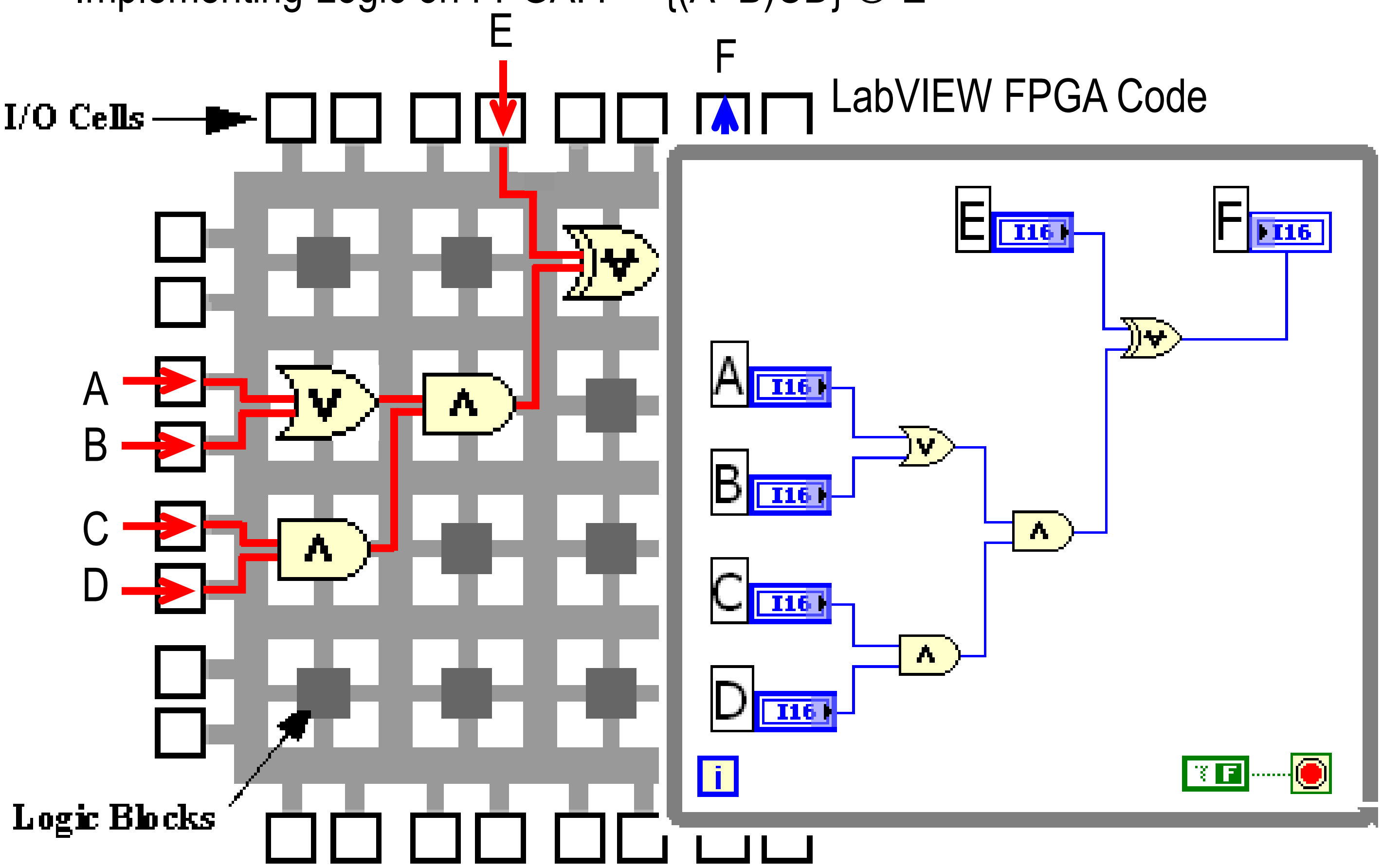


LabVIEW FPGA Tool Chain

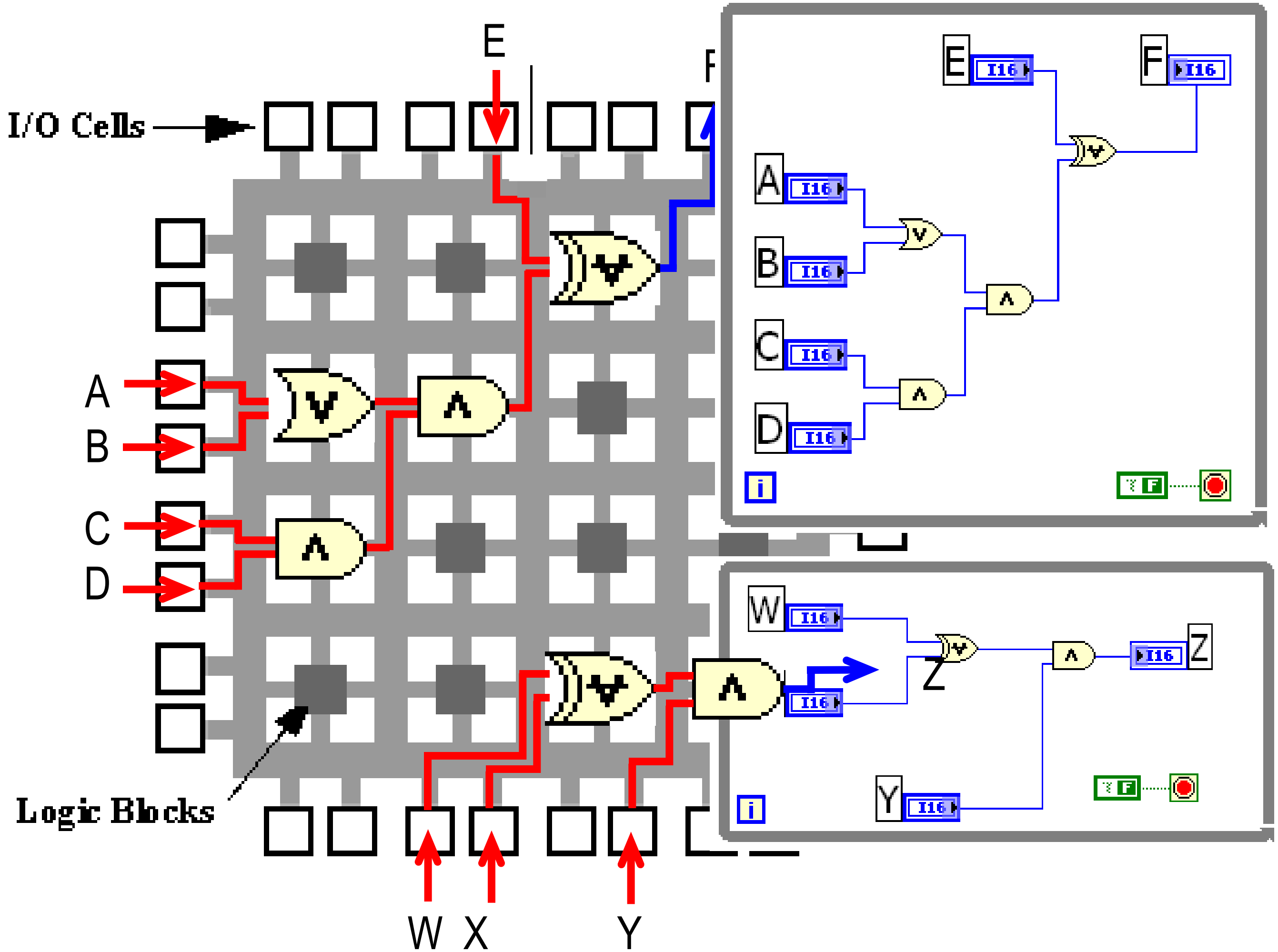


Simplified FPGA Example

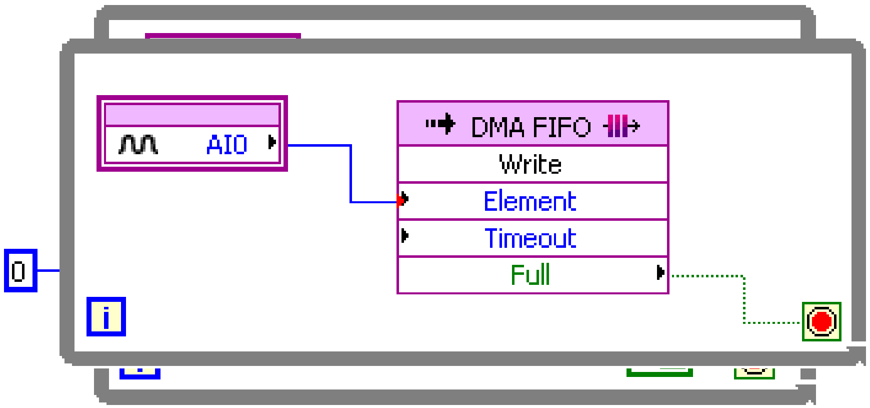
Implementing Logic on FPGA: $F = \{(A+B)CD\} \oplus E$

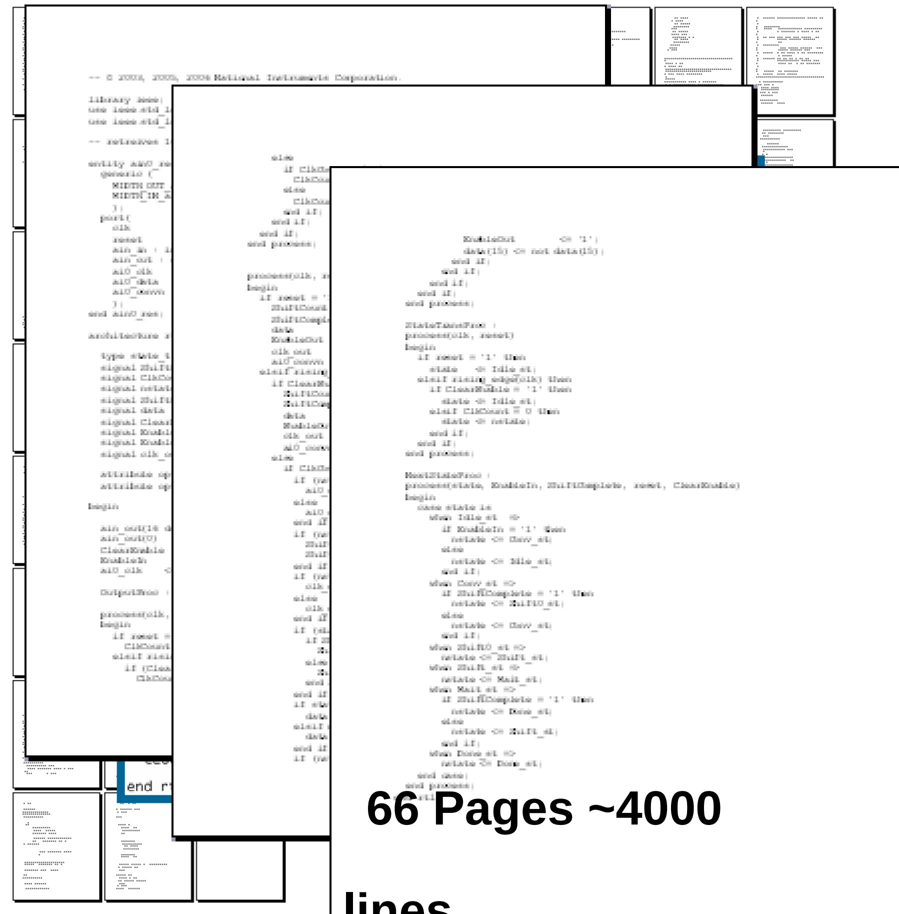


Simplified FPGA Example



LabVIEW FPGA vs VHDL





66 Pages ~4000 lines

Counter

Analog I/O

I/O with DMA

On-Board Processing and Data Reduction

Built-In I/O

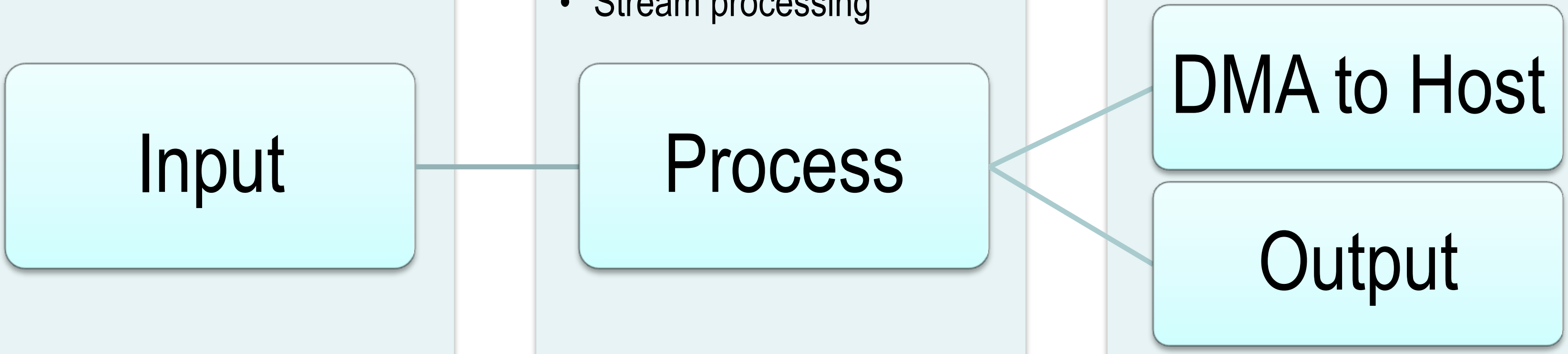
- Analog voltages
- Digital communications
- Sensor signals

Processing

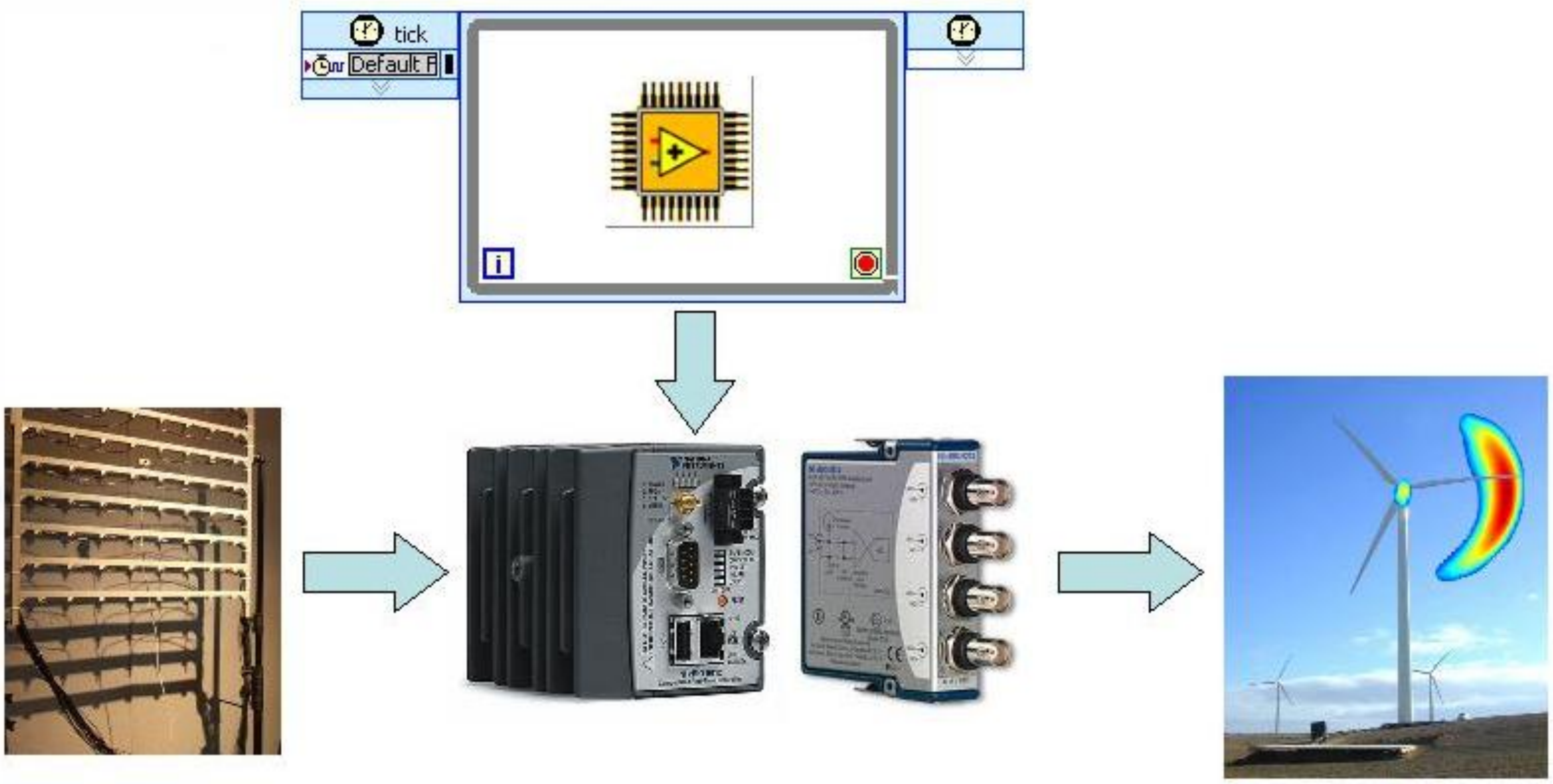
- Encoding/decoding
- Filtering/averaging
- Modulation/demodulation
- Decimation
- Stream processing

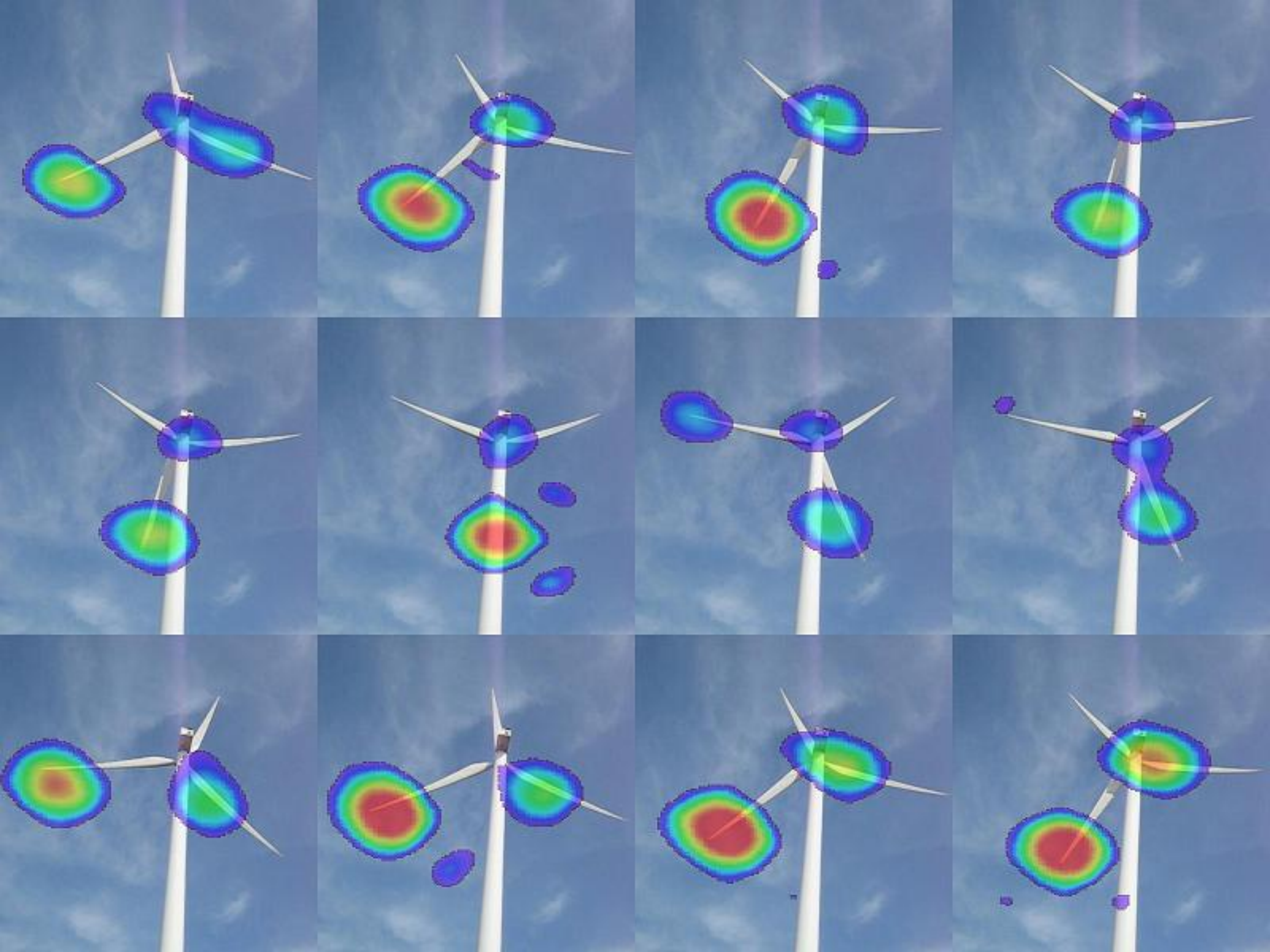
Output

- DMA preprocessed data
- Streaming from input to output without host involvement

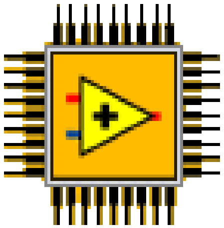


FPGA Real-Time Beamforming





Importance of FPGA in Systems



- ***High Reliability*** – Designs become a custom circuit
- ***High Determinism*** – Runs algorithms at deterministic rates down to 25 ns (faster in many cases)
- ***True Parallelism*** – Enables parallel tasks and pipelining
- ***Reconfigurable*** – Create new and alter existing task-specific personalities

FPGAs in Industry

Machine Control

- **Packaging/Processing**
  - High-speed motion control, batch control, discrete control
- **Heavy Machinery Control**
  - Real-time signal processing and control of power electronics, hydraulic systems
- **Semiconductor/Biomed**
  - Custom motion and vision inspection, material handling

Machine Monitoring

- **Machine Condition Monitoring**
  - Bearing order analysis, lubrication monitoring, cooling, combustion…
- **Mobile/portable DSA, NVH**
  - Noise, vibration, harshness, dynamic signal analysis, acoustics
- **Distributed Acquisition**
  - Central controller with distributed I/O nodes over Ethernet/wireless

In-Vehicle Data Acquisition

- **In-Vehicle Data Acquisition**
  - Automobiles, motorcycles, recreational vehicles, research aircraft, trains
- **Engine and ECU test cells**
  - HIL testing of engines and engine controllers, sensor simulation using FPGA
- **Rapid Control Prototyping**
  - Automotive/aerospace control prototyping