

Simulation of LIN Clusters for Reducing In-Vehicle Network Development and Validation Costs

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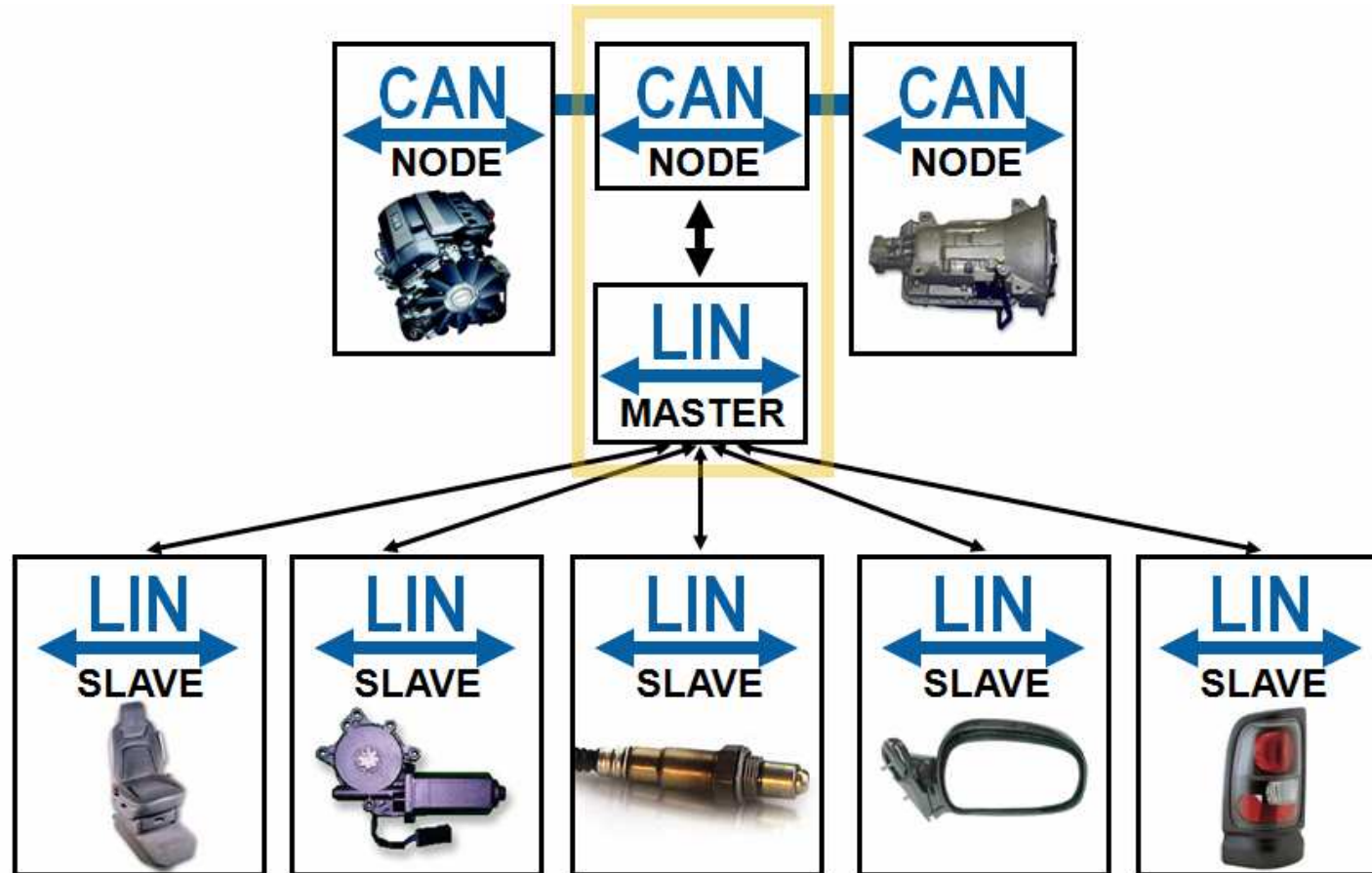
Embedded Networks Product Manager



Agenda

- LIN Overview
- Motivation
- Experimental Setup
- Simulation Topologies
- Questions

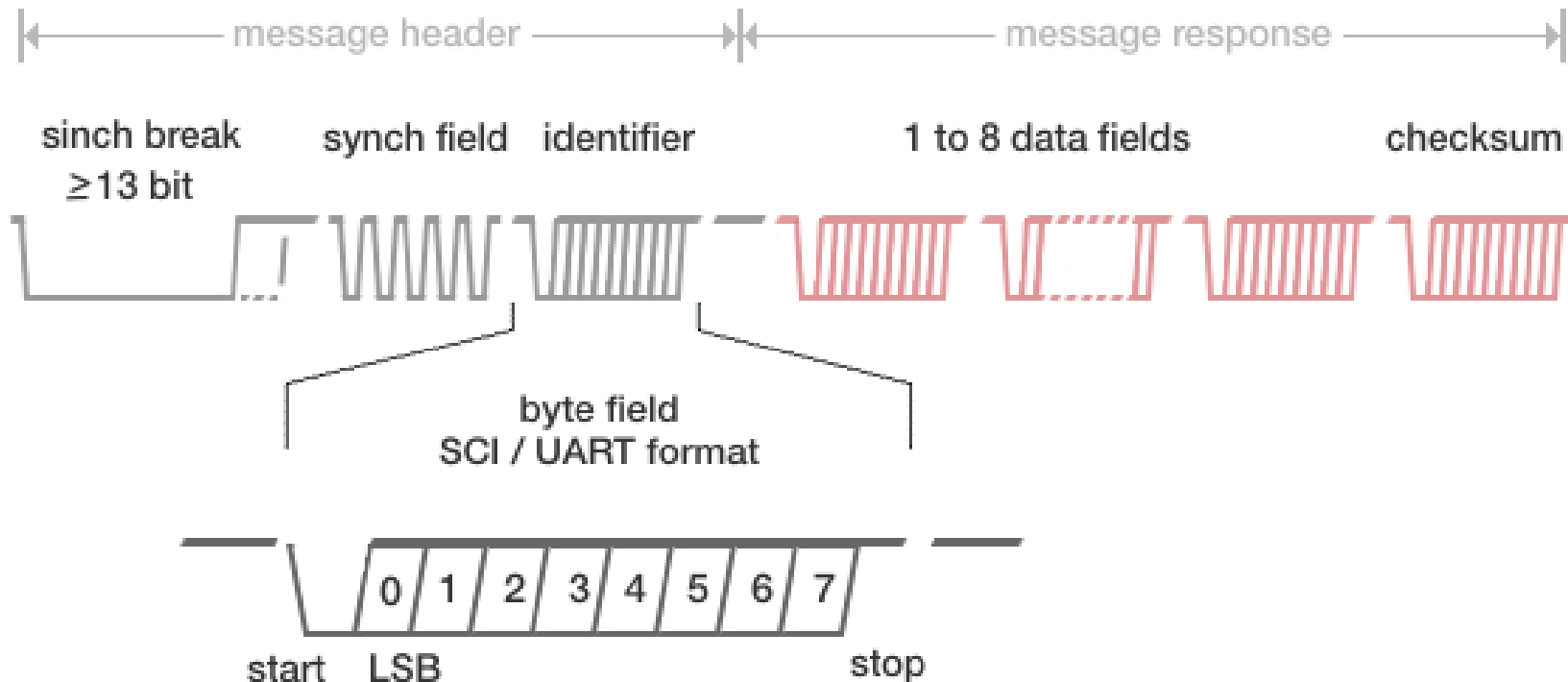
LIN Overview: Applications



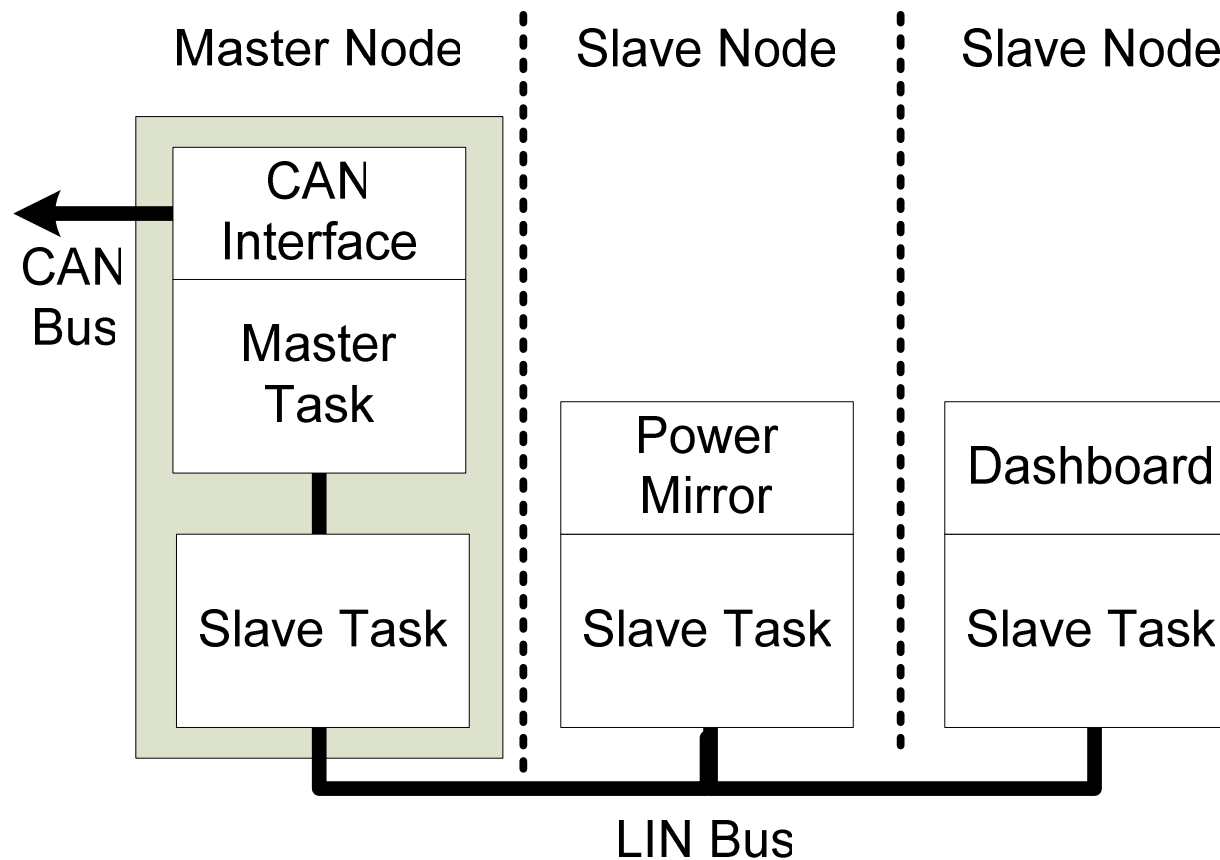
LIN Overview: Key Features

- Master/Slave
- Self-synchronizing slave nodes
- Multicast
- UART/ ISO9141 based
- Target Deployment Costs of \$.50-\$1 per node
- **Scheduled and deterministic**

LIN Overview: Frame Format



LIN Overview: Master-Slave Structure



Motivation

To create a simple, modular, simulation framework using off-the-shelf hardware to speed the testing and development of LIN Systems

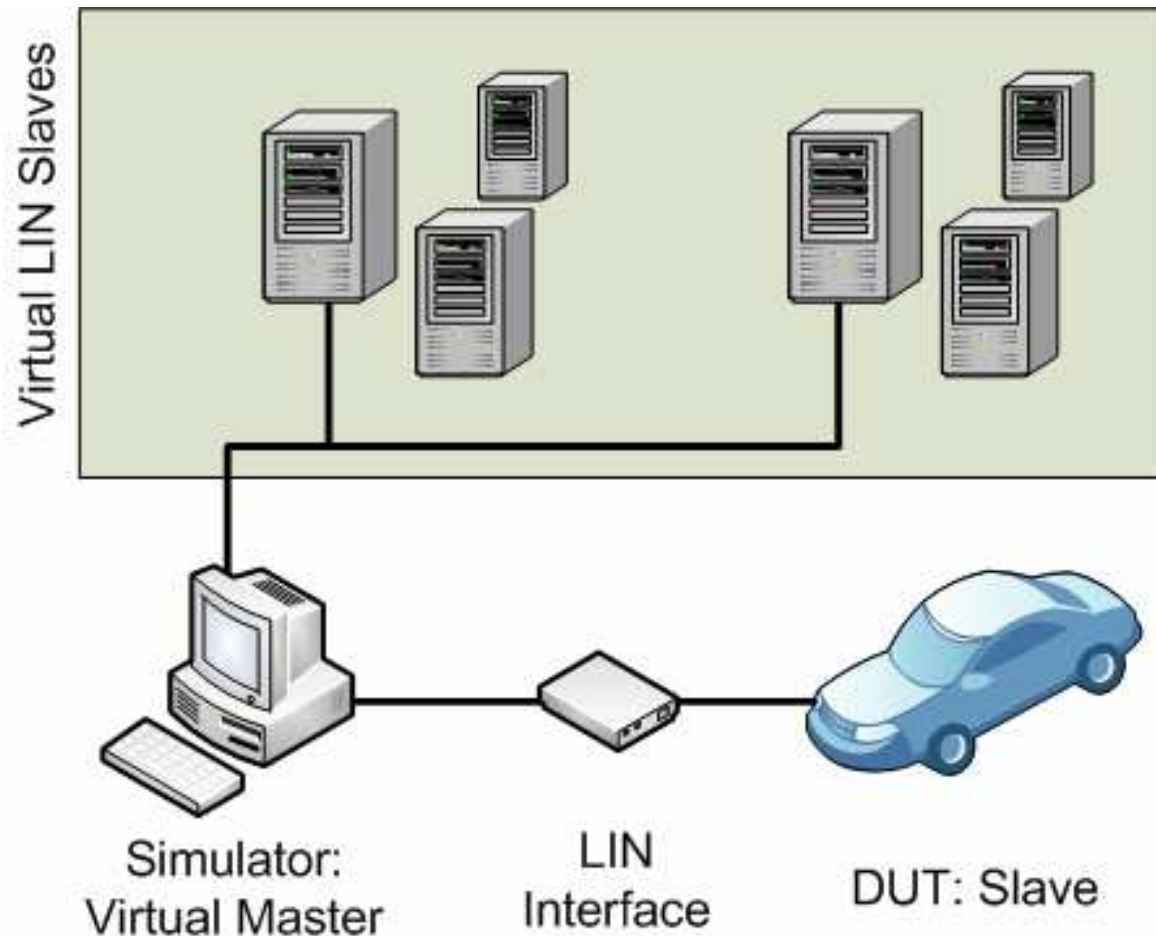
- Use simple and portable programming concepts
- Adaptable to a variety of LIN topologies
- Inexpensive to implement

Hardware Requirements

- Software access to LIN bus
- Ability to send and receive LIN headers and data *independently*
- Ability to continuously poll to read headers
- Selectable Master/Slave Termination
- Hardware Options
 - CAN or RS232 to LIN bridge
 - Any microcontroller with a UART and a LIN transceiver
 - USB/PCI/PXI to LIN interface

Simulation Topology #1

Restbus Simulation with Virtual Master and Slaves for **Slave Validation**



Simulation Topology #1

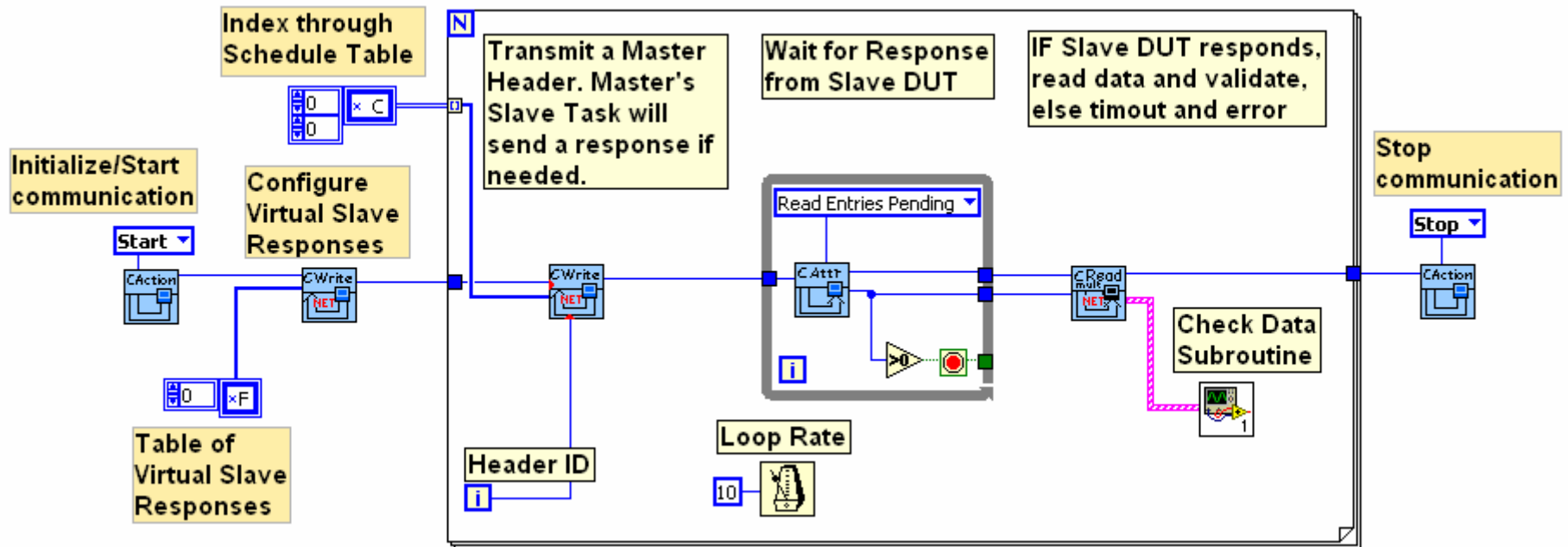
Restbus Simulation with Virtual Master and Slaves for **Slave Validation**

Publisher	Subscriber	Transmitted Data
Master Task	All Slaves	Master Update
Slave A	Master Slave Task	Data Frame A
Slave B	Master Slave Task	Data Frame B
Slave C	Master Slave Task	Data Frame C

Publisher	Subscriber	Transmitted Data
Virtual Master Task	All Slaves	Master Update
Virtual Slave A	Master Slave Task	Data Frame A
Virtual Slave B	Master Slave Task	Data Frame B
Slave C [DUT]	Master Slave Task	Data Frame C

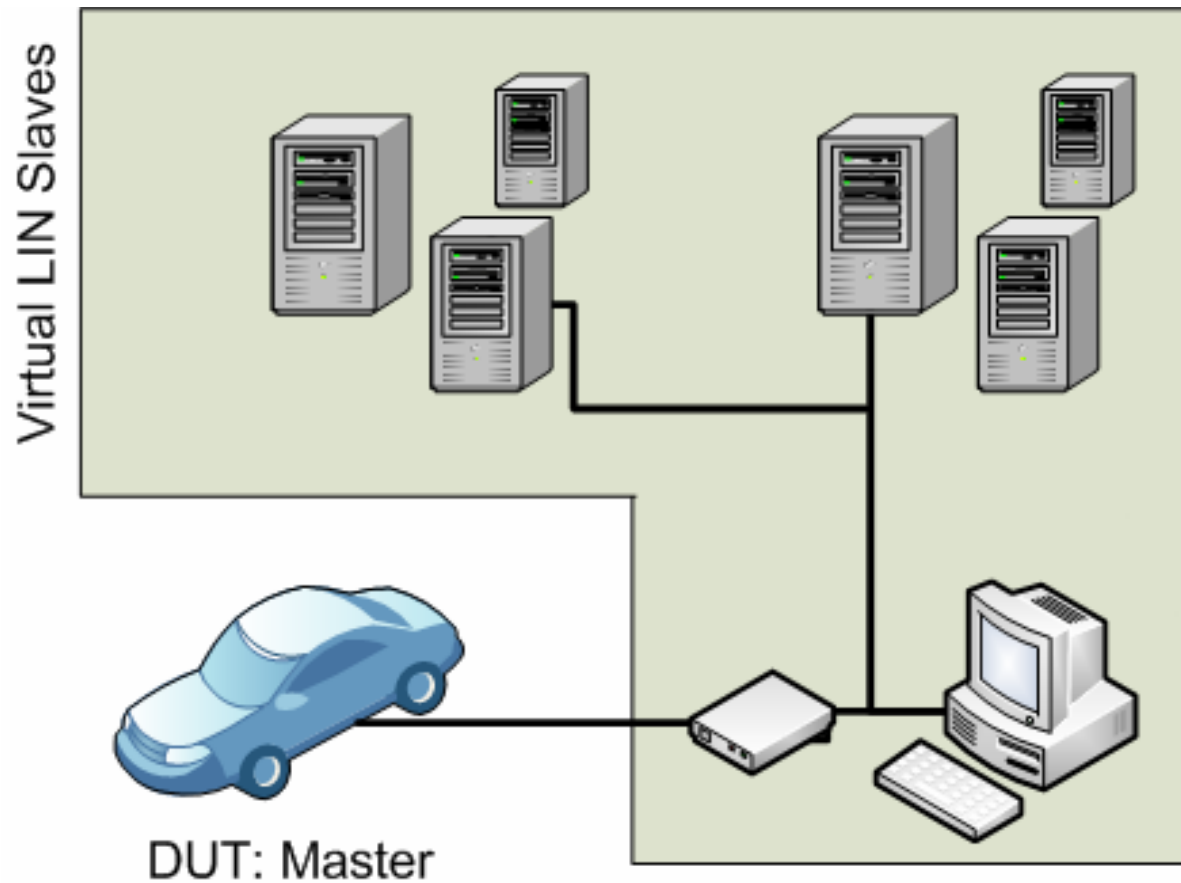
Simulation Topology #1

Software Model: LabView block diagram



Simulation Topology #2

Restbus Simulation with Virtual Slaves for **Master Validation**



Simulation Topology #2

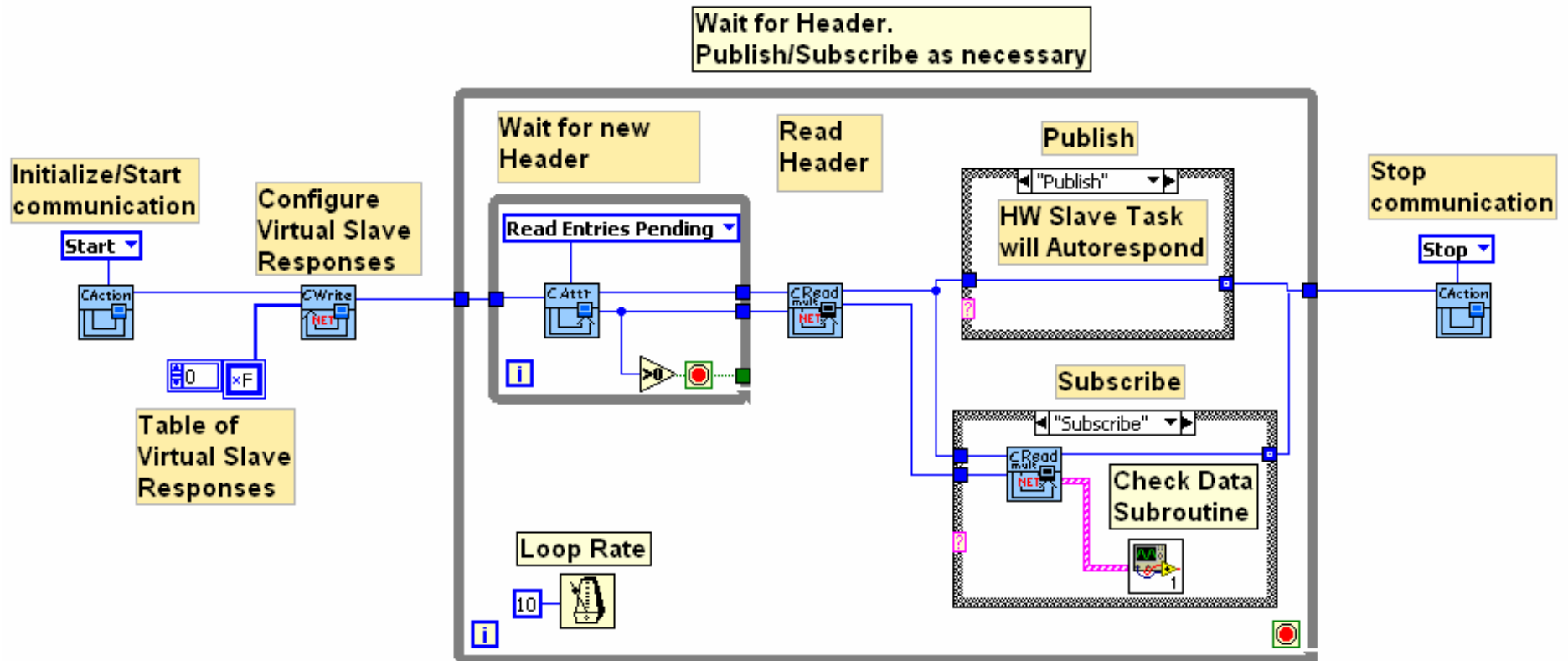
Restbus Simulation with Virtual Slaves for **Master Validation**

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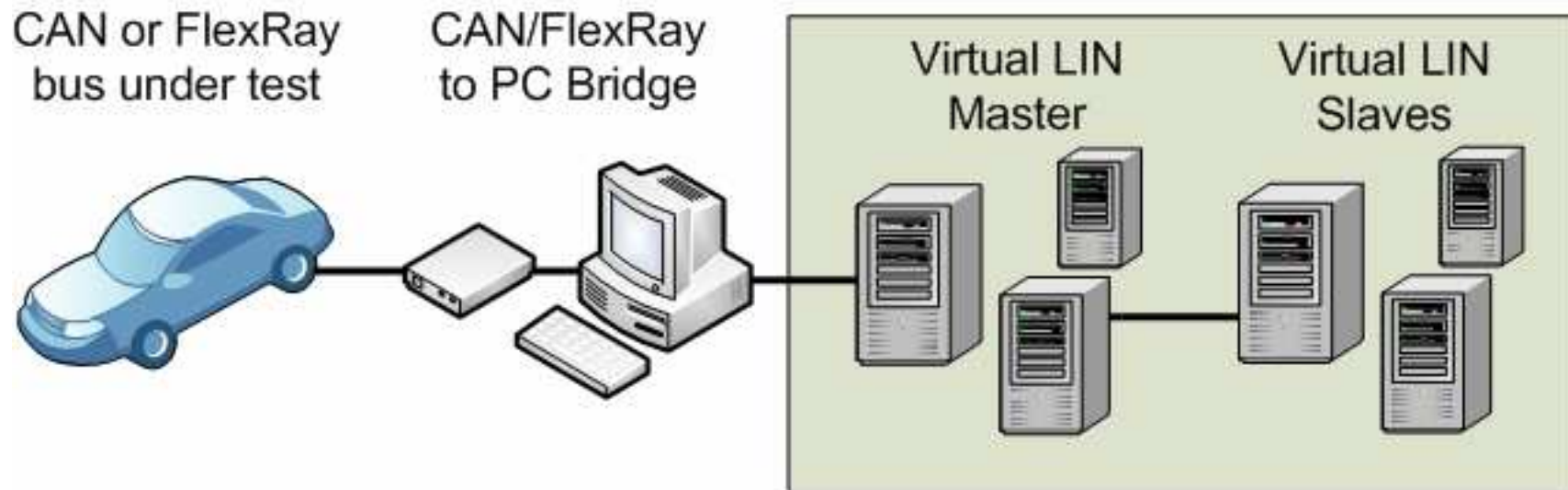
Simulation Topology #2

Restbus Simulation with Virtual Slaves for Master Validation



Extensions and Further Work

Fully Virtualized LIN for CAN/FlexRay Validation



Extensions and Further Work

- Add timing variation
 - Simulate extremes of bus timing in SW
 - Possible applications for LIN conformance testing
 - Implement using UART baud rate timing

Questions?